IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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MicroProbe Vx-MP Probe Card Technology

MicroProbe

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Overview

- Vx-MP Technology Key Features and Components
- Probe Design Considerations
- Key Performance Parameters
- Probe to Probe No-interference Confidence at Aggressive Bump Pitches
- Roadmaps
- Summary

Vx-MP Technology Key Features

- Combines Flexibility of MEMS probes installed in customer-specified x-y locations

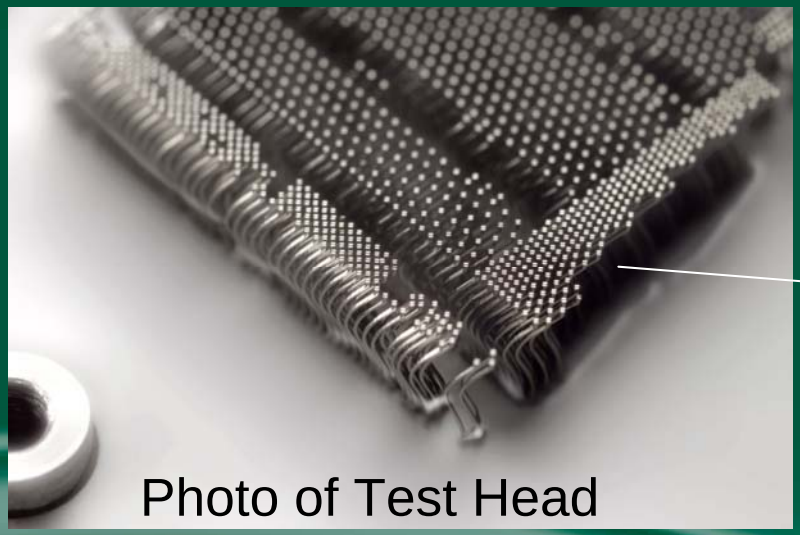
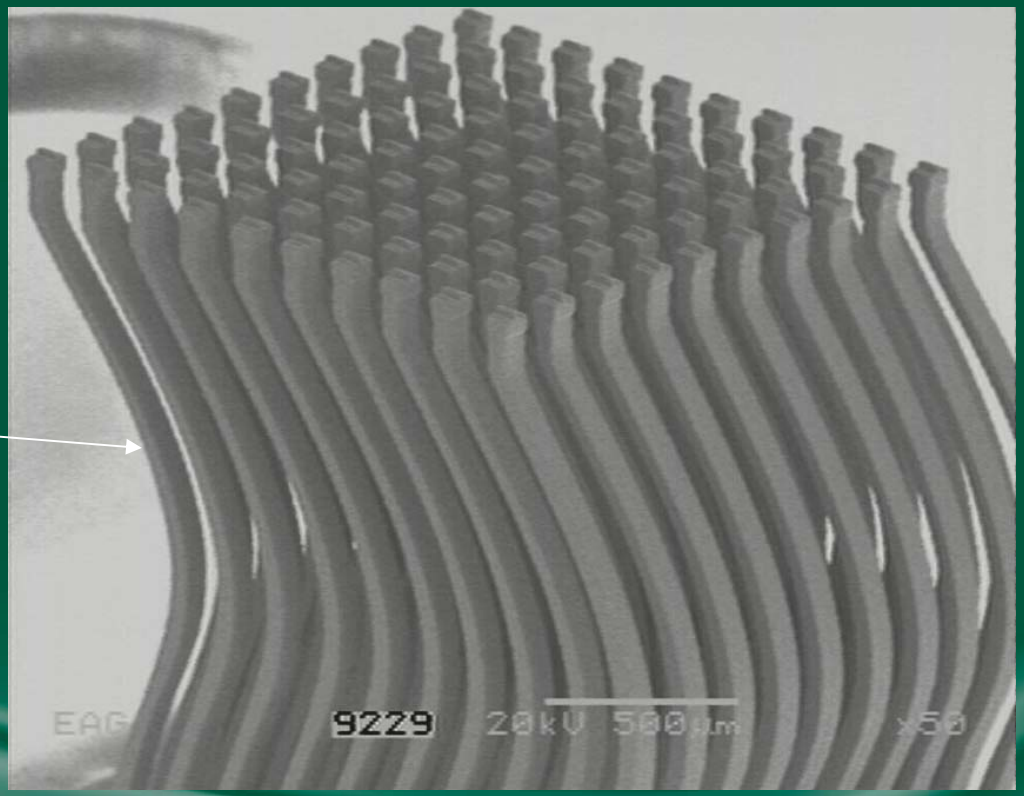


Photo of Test Head



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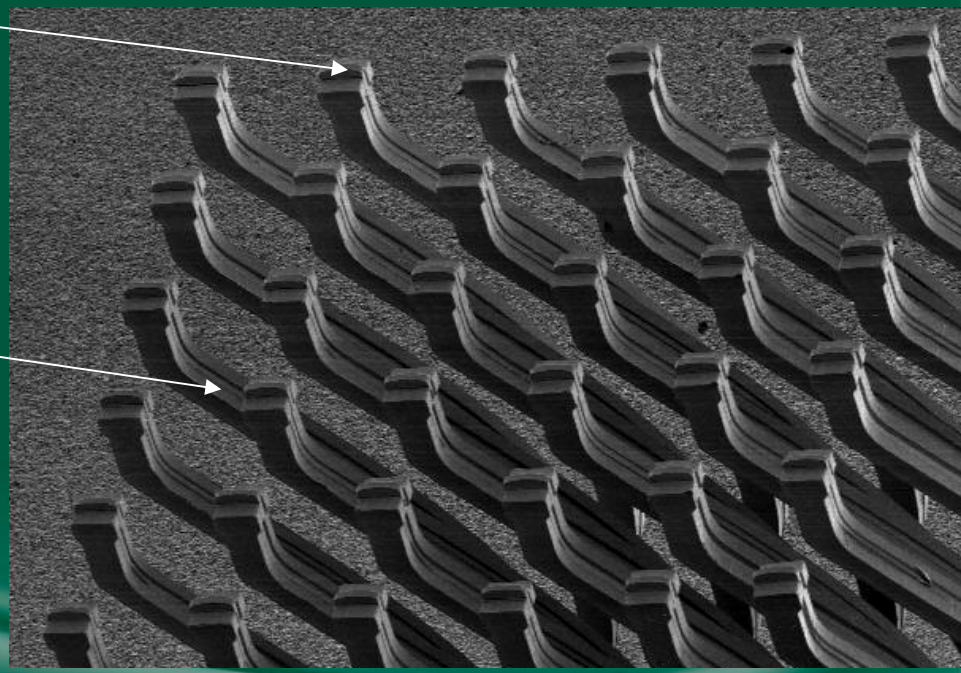
Vx-MP Technology Key Features

- Probes are fabricated utilizing 3-D photolithography-metal plating techniques
  - Probe tip – “skate” shape/material provides ideal contactor
  - Probe body material provides optimal spring action



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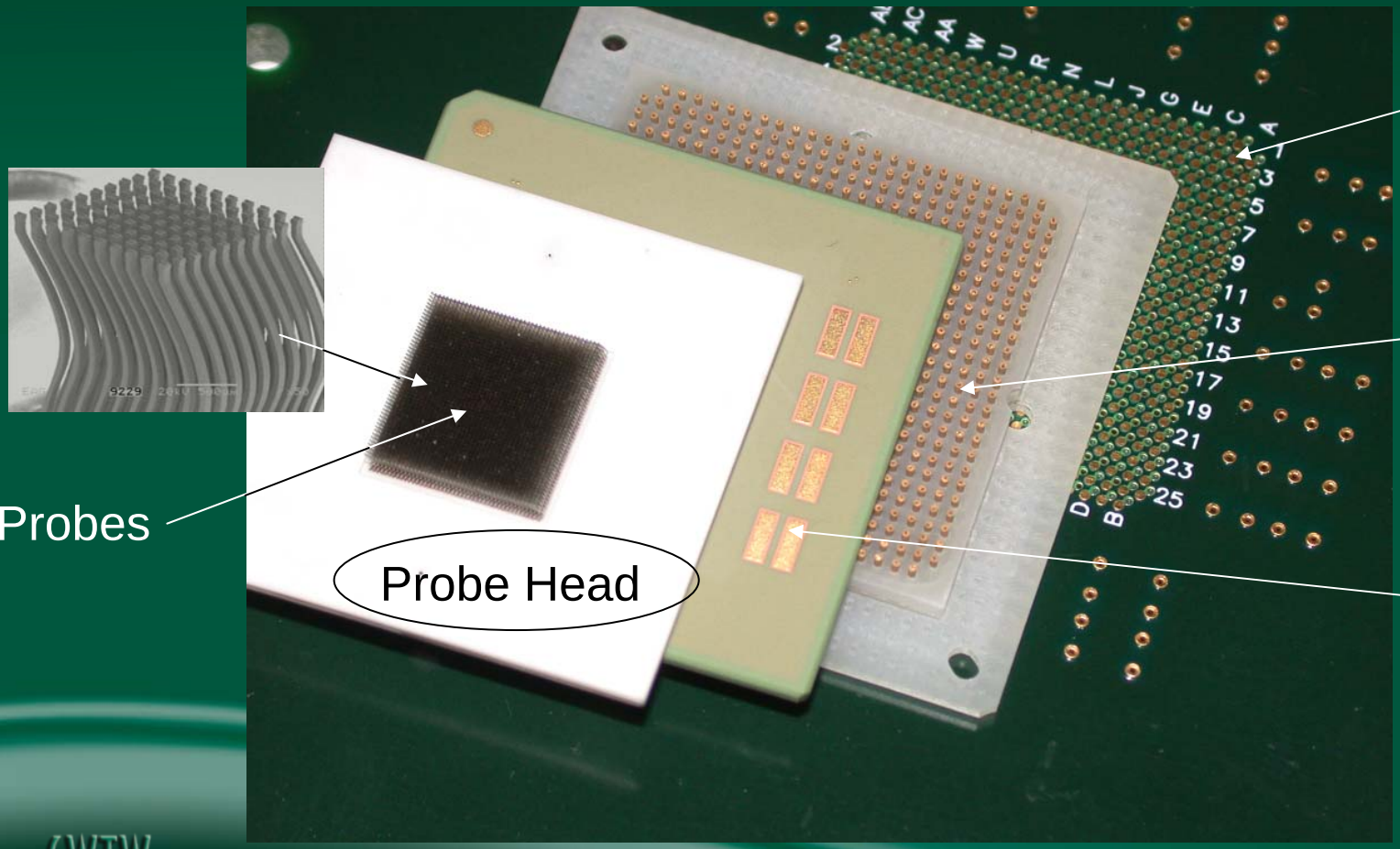
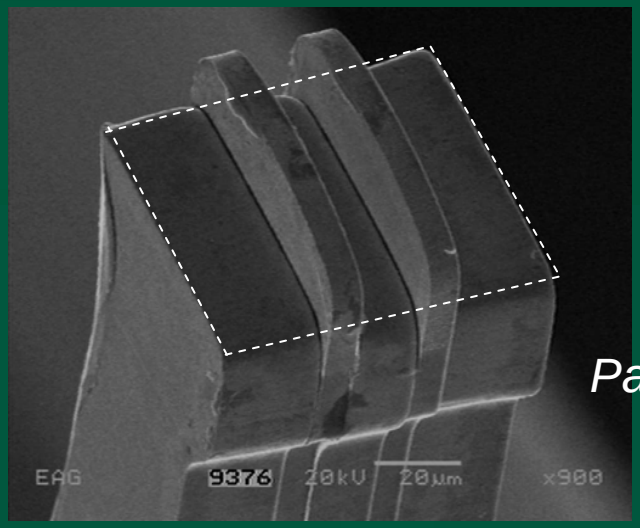
Vx-MP Technology Key Components



Vx-MP Probe Design Key Features

- Tip base provides stable target for prober alignment



Dual-Skate Probe Tip

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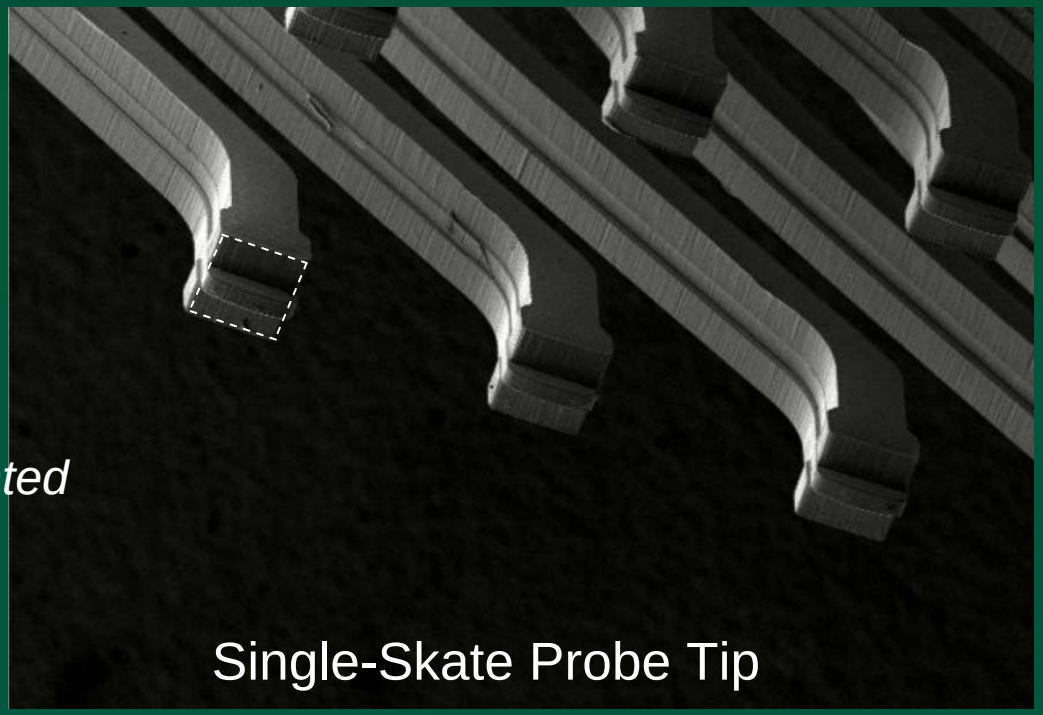
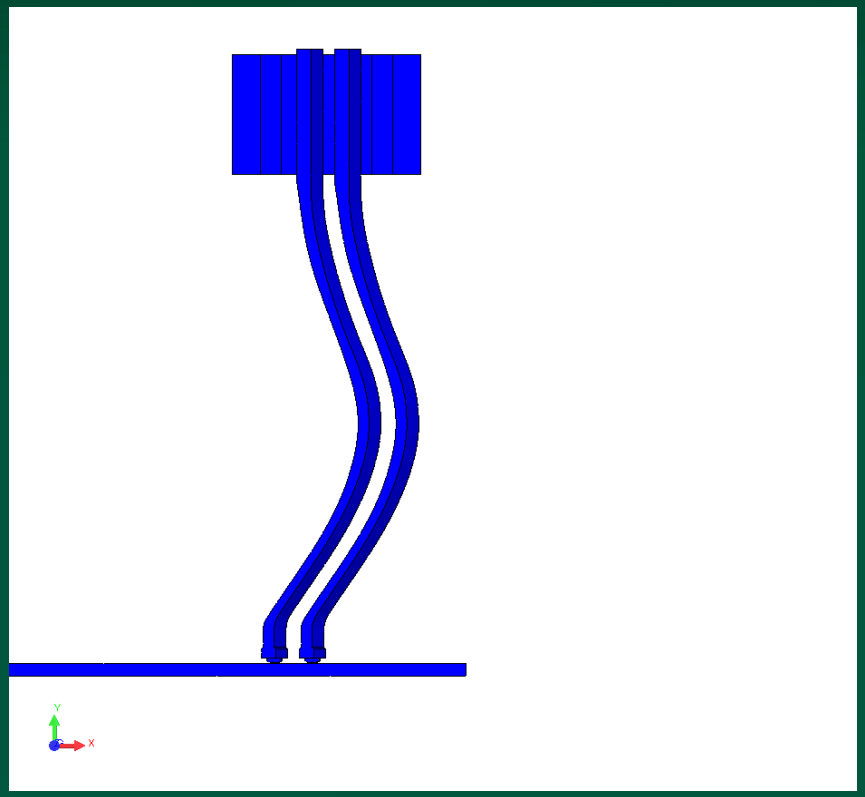


Single-Skate Probe Tip

Tip Base (flat)

Vx-MP Key Performance Features

- Vx-MP Probe Action



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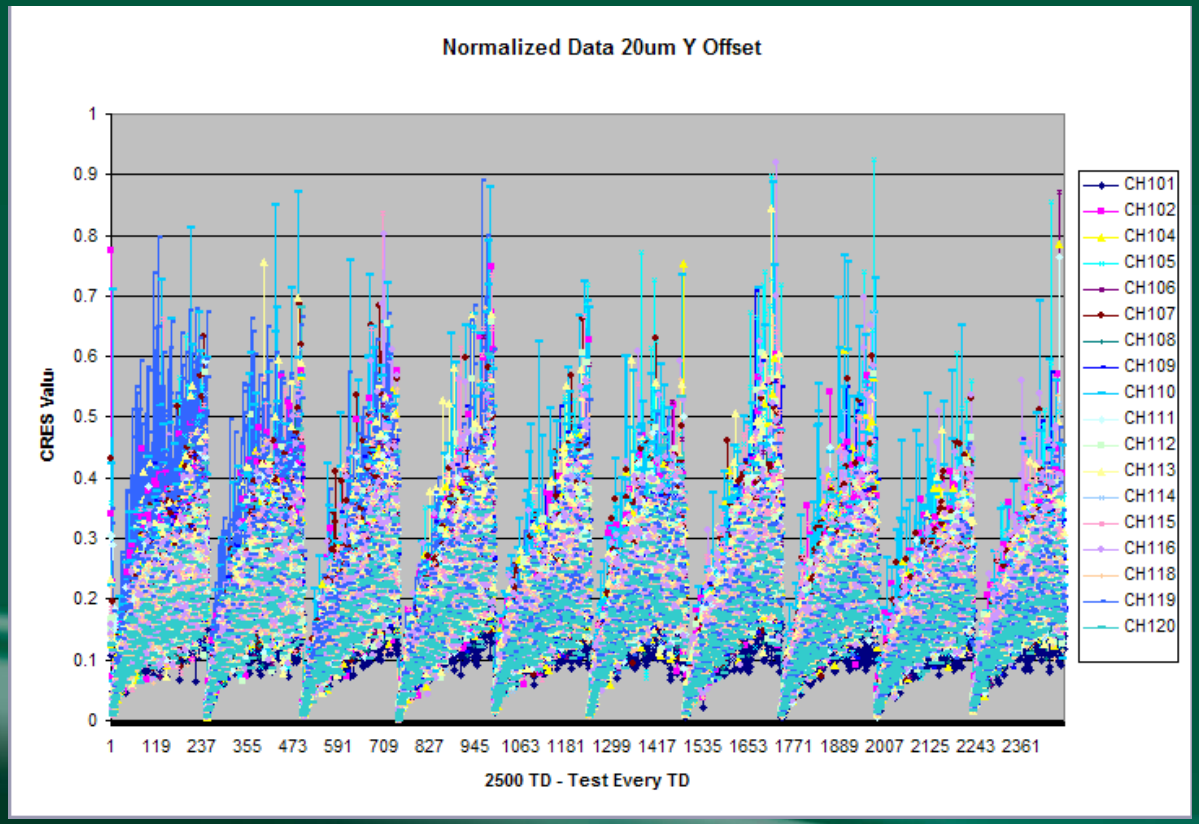
Vx-MP Mechanical Performance

- Vx-MP Probe Scrub Motion

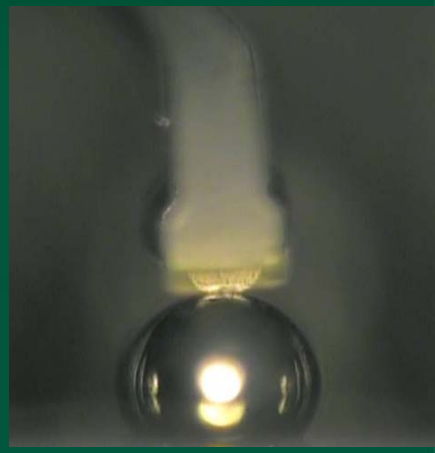
Patented

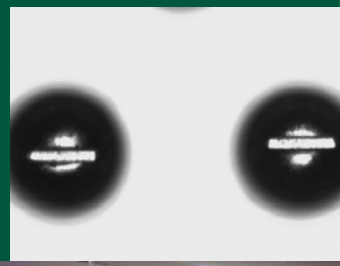
Vx-MP Electrical Performance

- Performance on Eutectic Flip-Chip Solder Balls, 400mA current prior to each measurement, 50 um Deflection
- 2500 TD, On-line clean cycle every 250 TD



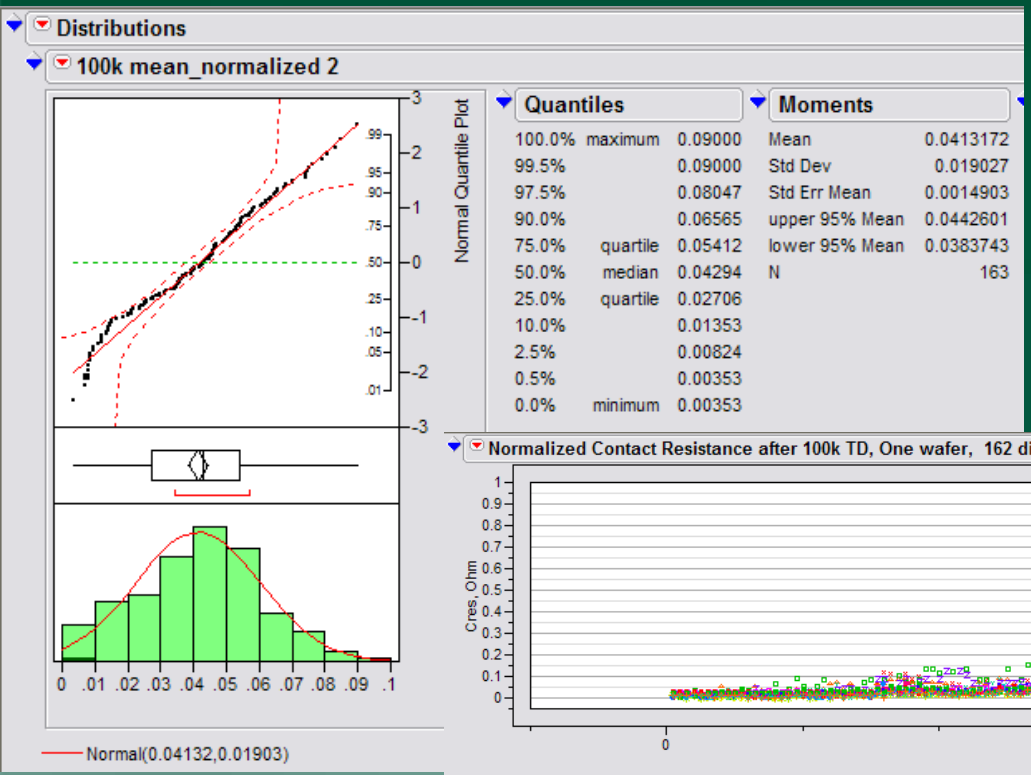
Contact Resistance Change, Ohm

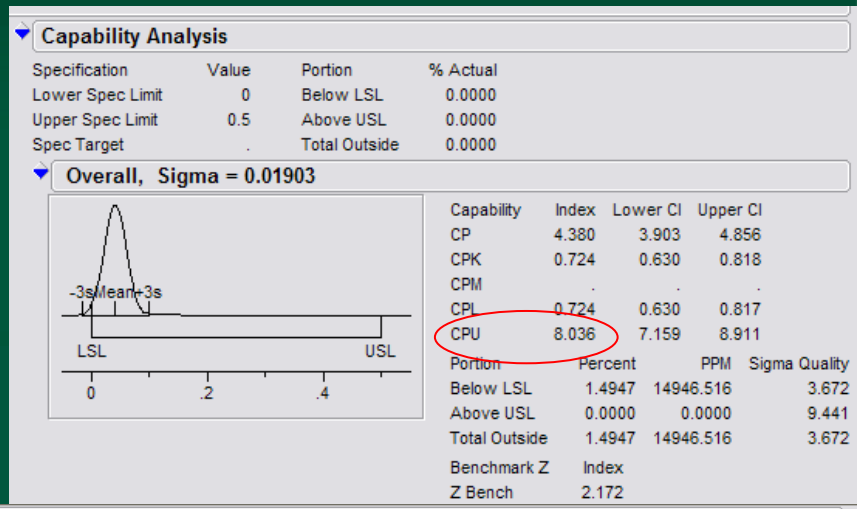


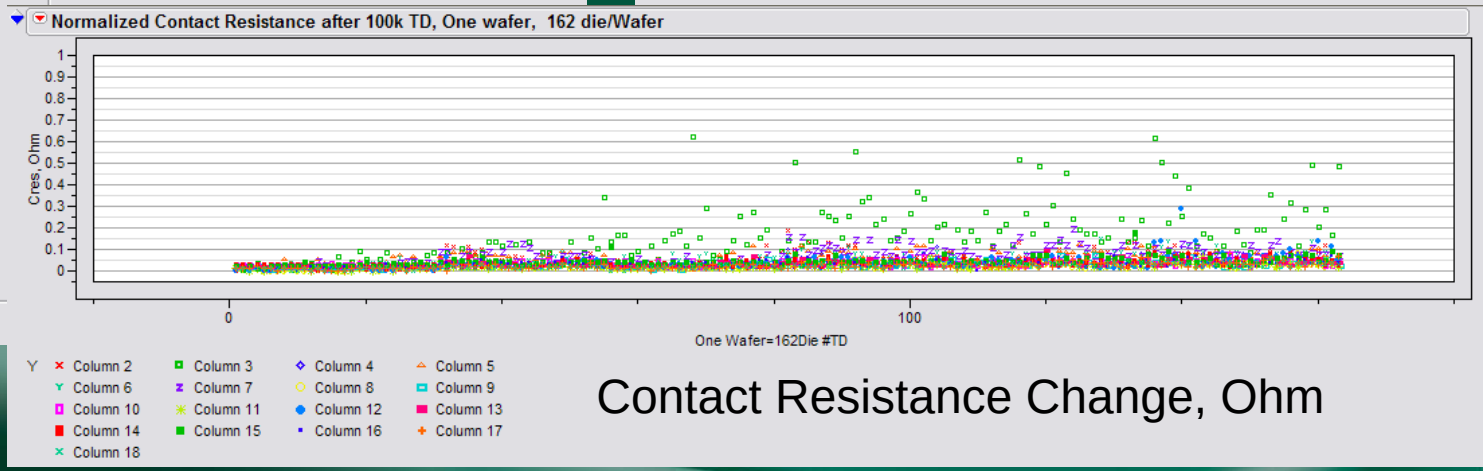


Vx-MP Electrical Performance

- Post 100k Touch Down Performance on 130um pitch on Copper @ 50 um Deflection



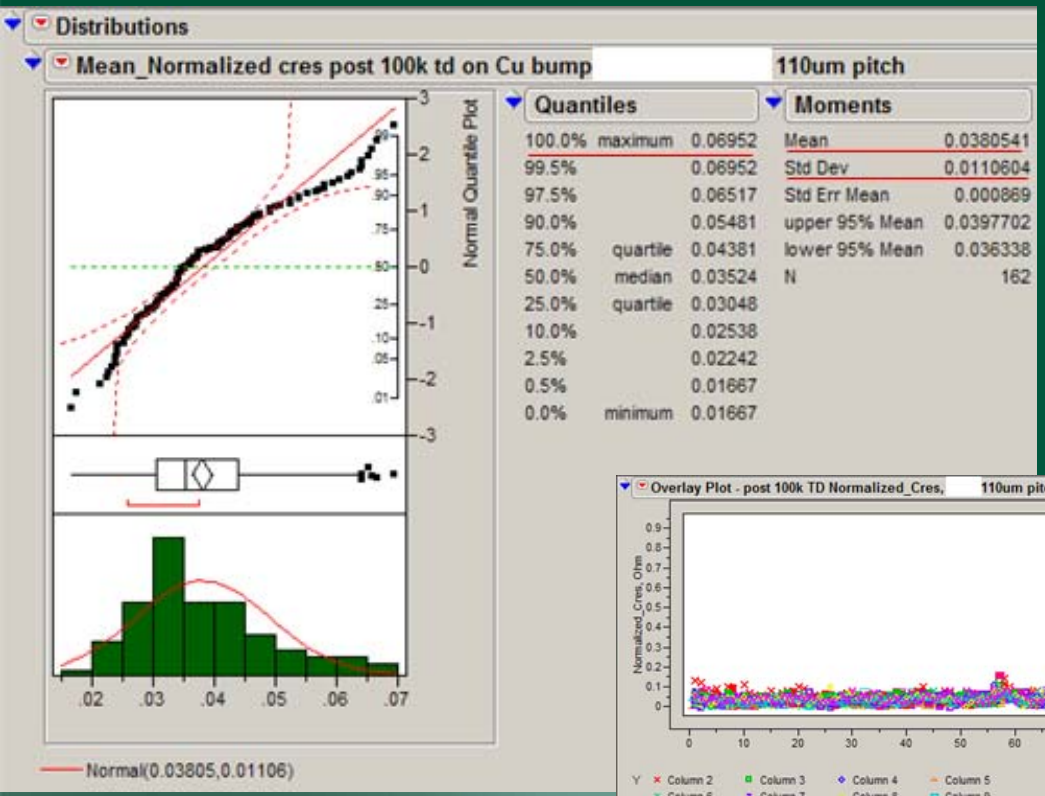


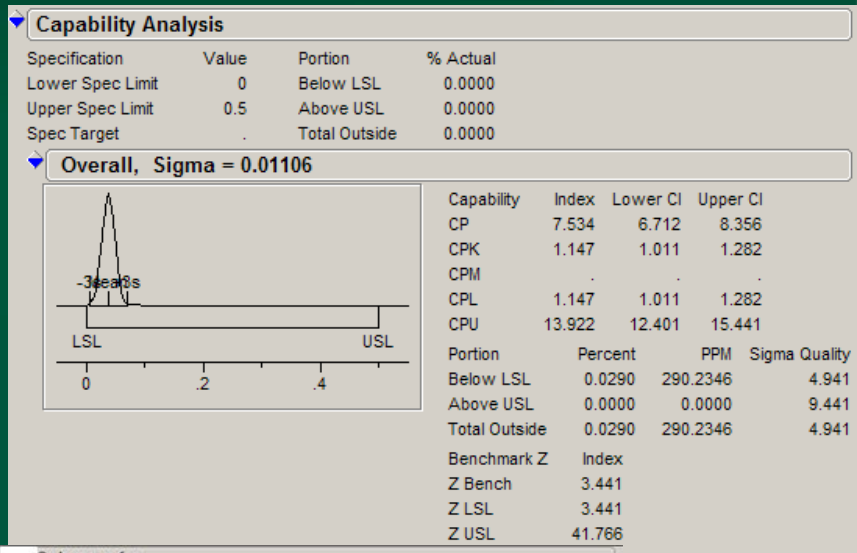


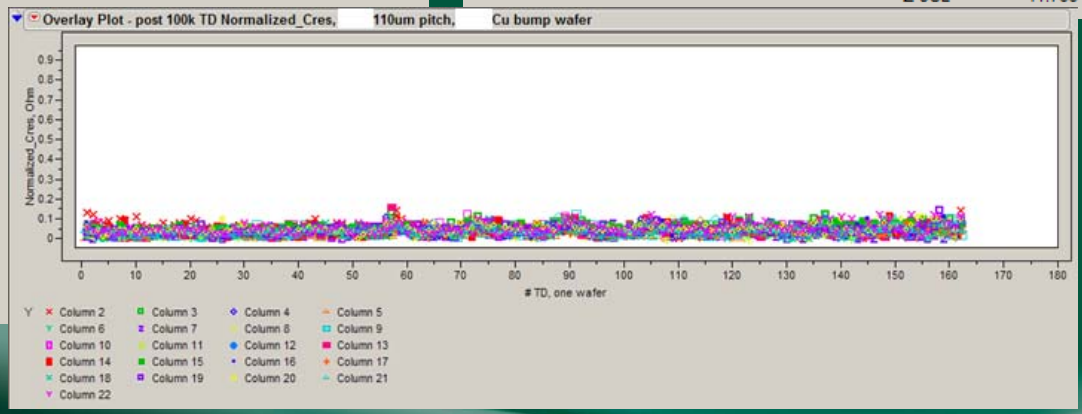
Contact Resistance Change, Ohm

Vx-MP Electrical Performance

- Post 100k Touch Down Performance on 110um pitch on Copper @ 50 um Deflection







Vx-MP Electrical Performance

- Contact Resistance Results on Copper
  - Cleaning performed prior to each wafer test

	CRES VALUE at INTERVAL, OHm			
	25k	50k	75k	100k
Mean	0.0190	0.0231	0.0284	0.0410
Std Dev	0.0046	0.0060	0.0162	0.0190
99.5% Quantile	0.0388	0.0418	0.0841	0.0900
100% Max	0.0388	0.0418	0.0841	0.0900
CPU @ 0.5 USL	34.8000	26.4000	9.6000	8.0000

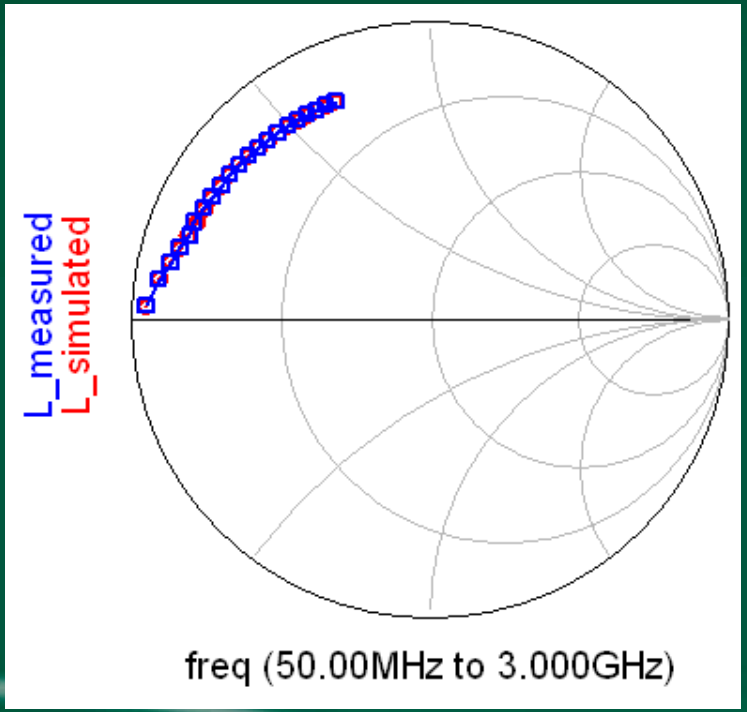
130um Pitch

	CRES VALUE at INTERVAL, OHm			
	25k	50k	75k	100k
Mean	0.0390	0.0450	0.0410	0.0380
Std Dev	0.0130	0.0150	0.0110	0.0110
99.5% Quantile	0.0820	0.0780	0.0770	0.0700
100% Max	0.0820	0.0780	0.0770	0.0700
CPU @ 0.5 USL	12.0000	9.9000	14.4000	13.9000

110um Pitch

Vx-MP Electrical Performance

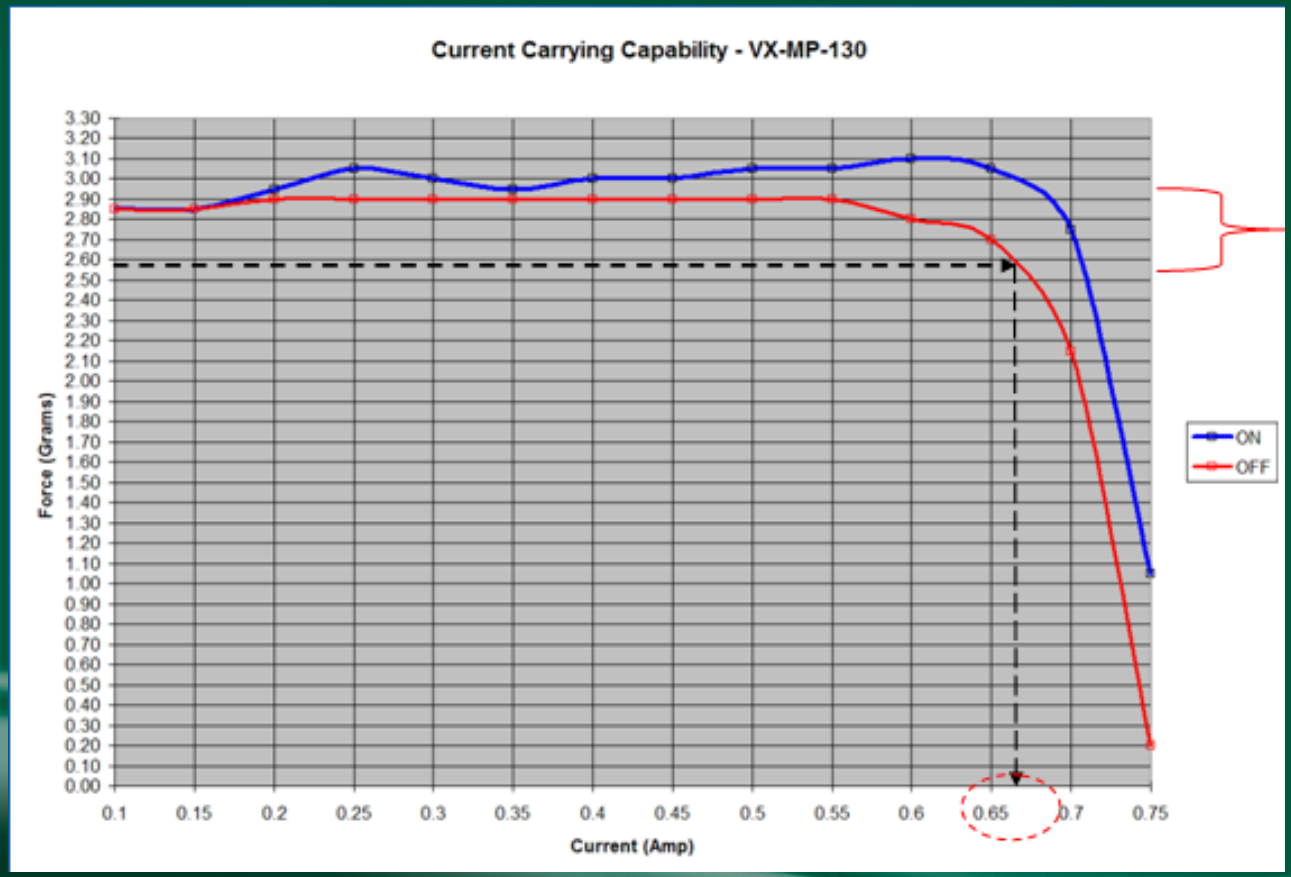
- Effective Inductance



	VX-MP-110	VX-MP-130
PITCH (µm)	L (nH)	L(nH)
110	1.64	x
130	x	1.32
215	2.1	x
245	x	1.92

Vx-MP Electrical Performance

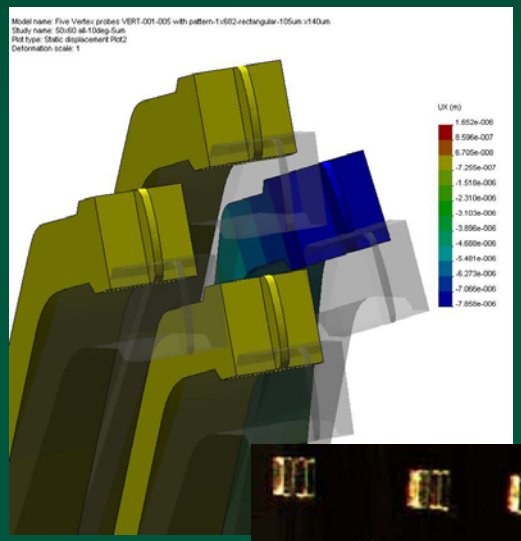
- CCC based on 10% CF Reduction under Steady State Current
  130 um Grid Array pitch Probe

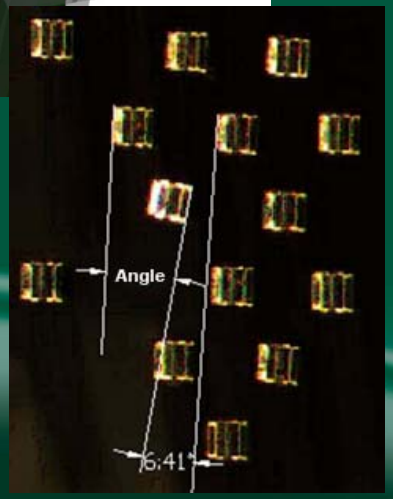


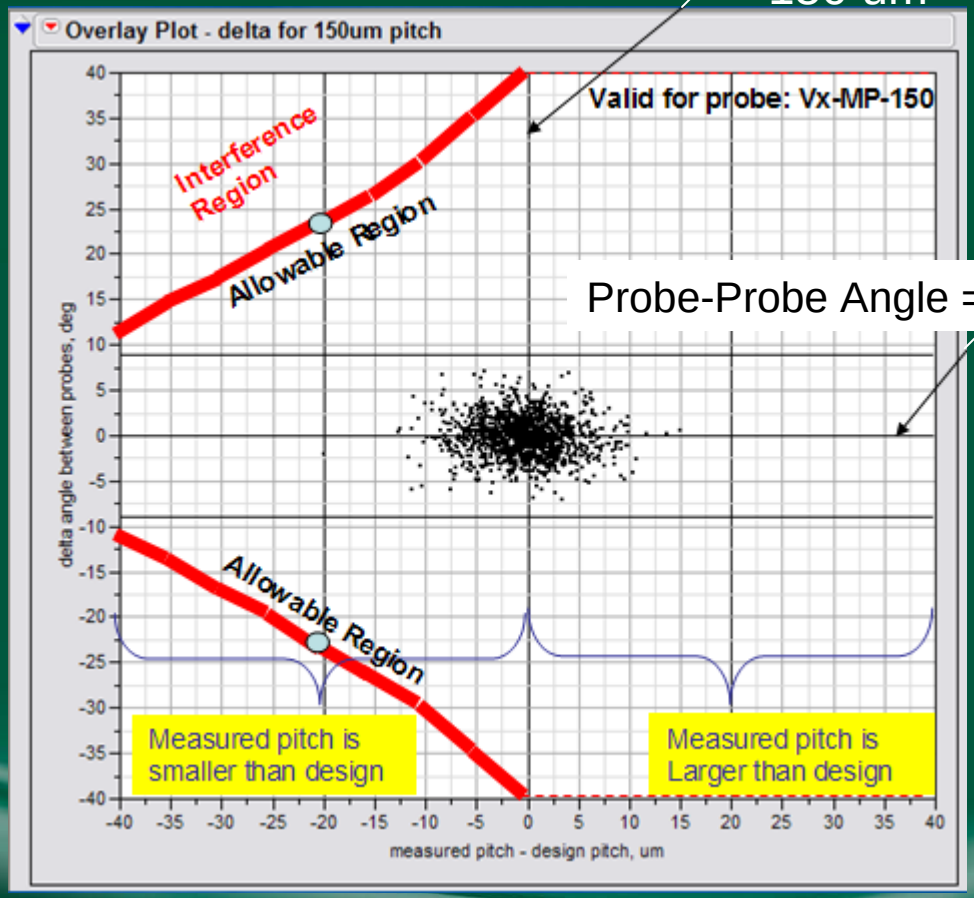
40um OT

Vx-MP Mechanical Performance

- Probe to Probe no-interference CPk = 3.6 @ 150 um pitch – for extreme bump height and scrub variation

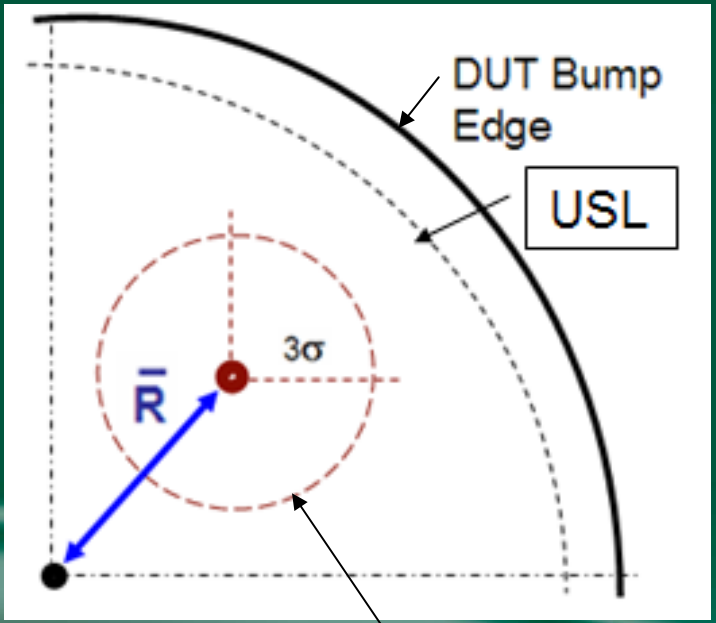




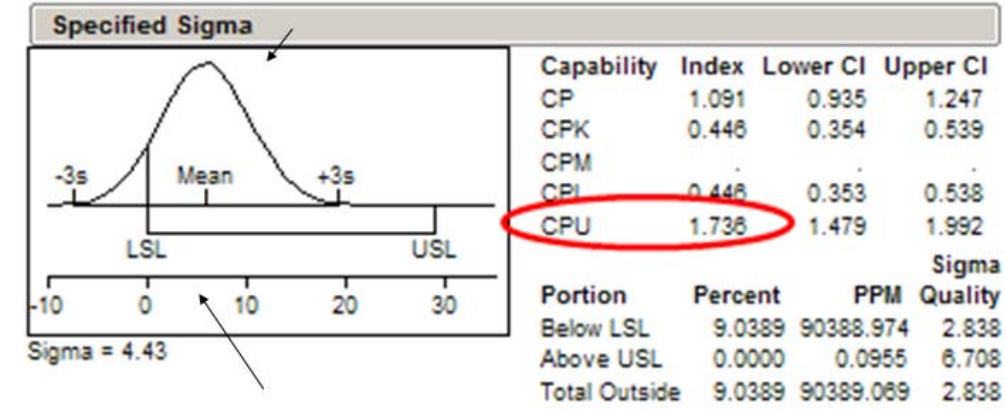


Vx-MP Tip-Bump Alignment Process Capability, CPU

- For 130um pitch & 90um nominal bump CPU= 1.74 Takes into account probe tip alignment and scrub motion



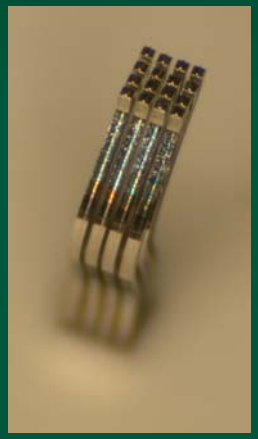
$$C_{pu} = \frac{USL - \bar{R}}{3\sigma_R}$$

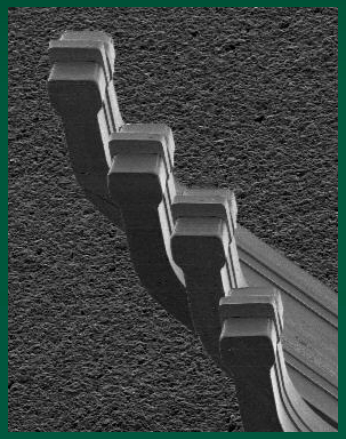


R=3*Stdev. Probe Tip location

Vx-MP Technology Pitch Capability Roadmap

- Vx-MP





	Full Grid Array								Peripheral single & dual Row			
Pitch	150um	140um	130um	120	110um	100um	90um	80um	70um	60um	50um	40um
	√	√	√	√	√	√	•	•	√	√	•	•

√ = Available Capability

• = Under Development

Summary/Next Steps

- Vx-MP technology platform combines accuracy of MEMS with flexibility of pre-made probes placed into customer specified x-y locations
- Addresses most aggressive wafer bump pitch roadmaps
- Tightly controlled scrub action optimizes electrical performance
- Next step: Larger footprint applications

Acknowledgements

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