A Membrane Probe for Testing High Power Amplifiers at mm-Wave Frequencies

Saswata Basu, Pat Nussbaumer, and Eric Strid
Cascade Microtech, Inc., 2430 NW 206th Avenue, Beaverton, OR, 97006, USA (503) 601-1000
TRW, One Space Park, Redondo Beach, CA, 90278 (310) 813-5618
saswata@cmicro.com eric@cmicro.com, Patrick_Nussbaumer@qmail4.nba.TRW.com

Topic No. 13 Application Oriented

ABSTRACT

Traditional coaxial-needle probe cards have difficulty in incorporating combiner structures and generally have poor bypassing capability at high frequencies. In this paper, we will demonstrate how membrane probes can incorporate these features with minimal parasitic effects and conduct accurate and fast testing of power amplifiers at Ka-band.

Introduction

There are two principal problems that traditional coaxial-needle probes face with high power amplifier chips tested on-wafer. One is the difficulty of implementing off-chip matching networks on coaxial probes due to significant parasitics associated with assembly at high frequencies. The other problem is the inability to provide an RF short for the DC lines close to the probe tip. Besides these shortcomings conventional coaxial-needle technology is mechanically not as robust; it requires careful handling and is ill-suited for a production type environment. We will show how a membrane probe [I] can integrate combiners with minimal parasitic effects and conduct accurate and fast testing of Ka-band power amplifiers.

The power amplifier is a two-stage PHEMT device designed and fabricated by TRW. The device has two 50 ohm inputs and four 36 ohm outputs. The testing specifications for this chip require a 2-by-l splitter at the input and a 4-by-l combiner at the output with current carrying capability of 2 A.

Probe Description

The layout of the probe is shown in Figure 1. It consists of an input circuit on the left and an output circuit on the right with symmetrically located DC bias lines on the top and bottom. The input circuit has a Wilkinson splitter with its legs having a characteristic impedance of 72 ohms to match the 50 ohms at the tip. The microstrip lines have a solid ground backing unlike the output circuit where it is meshed. The solid ground plane is removed at the resistor pad locations to keep the characteristic impedance close to 50 ohms. The resistors are thin film resistors on alumina substrate and have 20 x 6 mils physical dimension. At the edge of the layout the microstrip goes through a CPW transition to interface the center rectangular ring of the probe card. The transition between the probe and the card is iterated to insure a controlled impedance of 50 ohms over 50 GHz.

The output circuit unlike the input is based on meshed ground because the RF lines need to accommodate 2 A of DC current. The meshed microstrip line can be represented by an inductor and capacitor network. The areas of the line with no ground bar underneath are inductive whereas the portions with the ground bar component of the mesh under the line are capacitive. Because of the apparent fragmentation of the ground, signal lines can be made wider without any change in the characteristic impedance while accommodating larger amounts of current. The width of the lines for this specific design are derived from subsequent measured results on test structures.

The output circuit has a 4-by-l combiner with its front legs (closest to the tip) having characteristic impedances of 60 ohms to match the tip impedances of 36 ohms. The bias networks consist of two quarter-wave lines at the center frequency. The ground mesh is removed from the first line to increase its characteristic impedance, and the radial stub has a ground plane to maximize its capacitance. A DC blocking cap is mounted at the edge of the output RF...
line; the ground underneath the mounting pad is removed to eliminate any parasitic capacitive effect on the transmission line.

The other DC bias lines are made wide to lower their characteristic impedance. The 150 pF bypass capacitors are mounted close to the tip of the probe to provide a good RF short. An equivalent circuit looking into one of the DC lines would see a pi circuit with the short transmission line capacitance, the ribbon inductance, and the 150 pF. By controlling the width of the lines and the distance of the bypassing capacitor, stray inductances can be lowered to less than 0.5 nH. This bypassing capability is lower by a factor of 20 relative to conventional needle card technology.

The input and output circuit of the probe is characterized using a custom impedance standard substrate (ISS). The ISS was laid out to accommodate load and short standards for the input and the output circuit at Ka-, Q-, and V-band for TRW’s respective PHEMT amplifiers. The load standard is made to match the footprint of the probe bumps and the impedances of the input and output circuit. The characterizations of the circuits are made by calibrating up to the coaxial cable, attaching it to the probe, and then measuring three known standards such as open, short and load. Considering these three measurements and the assumption that S21=S12 the three s-parameter unknowns can be determined. One such characterization is that of the output circuit as shown in Figure 2. The return and insertion losses are below 10 dB and 5 dB, respectively, in the 32-34 GHz range. Most of the circuit losses are in the membrane probe and are predominantly conductor losses.

Results

There are various different calibration schemes that can be used to test the TRW Ka-band chips on-wafer. The simplest and most efficient one chosen was a response thru calibration to determine the insertion gain of the amplifier. This was an adequate measurement criterion for the production testing of these chips for known good die. We fabricated a custom matching thru between the input and output circuit on membrane and mounted it on a glass slide. The loss and delay of the thru were measured and calculated independently with a pair of ACP probes and entered into the calibration. The comparison between probe and fixtured data is shown in Figure 4. The two curves correspond quite well showing the viability of on-wafer testing scheme using this membrane probe. The curves seem to be shifted in frequency by about 0.5 GHz. This is attributed to the difference in parasitics of bond wires in the fixtured set-up relative to the bumps and lines at the tip of the probe. We will investigate this testing scheme further for higher frequency applications such as in the Q and V band.

Conclusions

We have shown the viability of integrating combiner circuits in the membrane probes for testing power amplifier chips at Ka-band at on-wafer level. Such integration reduces parasitics that are significant at very high frequencies and enable fast production level testing.

References

Figure 1: A Ka-band membrane probe for testing PHEMT amplifiers with two inputs and four outputs at non-50 ohm impedances.

Figure 2: An impedance standard substrate (ISS) designed to calibrate the membrane probe in Figure 1.

Figure 3: S-parameter responses of the output circuit of the membrane probe in Figure 1.

Figure 4: Comparison of measured responses between membrane probe and fixture set-up of the TRW Ka-band amplifier.