For Designers at Higher Frequencies

Microwaves & RF

Test & Measurement Issue

News
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Design Feature
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Product Technology
Power meters offer flexible test capabilities

Probes check multifunction RF ICs
COMPLEX integrated circuits (ICs) can provide many functions in a small space. These same benefits that allow engineers to shrink portable and wireless designs also make it difficult to perform at-speed, on-wafer testing of these ICs. Fortunately, Pyramid Probe™ cards from Cascade Microtech (Beaverton, OR) provide a solution for at-speed, on-wafer testing of high-speed analog, digital, and mixed-signal ICs.

At-speed wafer probing is essential for delivering known good die, increasing wafer yield, or for prompt fabrication-process feedback. In engineering development, at-speed wafer probing can reduce the time to market by shrinking the design-fabricate-test cycle time. The time-consuming and sometimes destructive dicing and packaging steps required for functional testing are eliminated. The immediate and specific feedback received from wafer testing speeds the redesign efforts. In addition, more and more complex systems are using dense flip-chip bonding of die in multichip modules (MCMs). Improved performance and cost through increased silicon efficiency require functional die sort to minimize rework and scrap. In some instances, a single bad die bonded into an MCM can result in scrapping the entire module.

How is high-performance functional testing accomplished on-wafer? The electrical performance of electronic packaging must be equaled if not surpassed by a probe capable of making hundreds of thousands of consistent and repeatable contacts on die with as many as 500 to 1000 bonding pads. Traditional epoxy-ring needle-probe cards become impractical over approximately 500 pads, with frequent maintenance required to maintain needle planarity and pad alignment. Electrically, the needles exhibit high inductance and inductive coupling. A typical ground or power needle will have 10-20-nH inductance. At the relatively-low frequency of 2 GHz, crosstalk as high as 10 dB, insertion loss of 3 dB, and a return loss of only 5 dB are typical.

A summary of at-speed wafer probing (Fig. 1) shows the types of probe bandwidths, clock speeds,
2. This wafer side view shows the membrane core of a Pyramid Probe card. A single nickel-alloy contact bump is shown in the inset.

and rise times that are necessary for different applications. Chip complexity is on the vertical axis and speed/frequency is on the horizontal axis. Simple device characterization ranges to more than 100 GHz for some pseudomorphic-high-electron-mobility transistors (PHEMTs) and GaAs heterojunction bipolar transistors (HBTs). Analog and mixed-signal RF and microwave ICs also are wide-ranging in bandwidth with increasing complexity—it is not extraordinary to have a single IC with 40 high-speed signal paths.

At the other extreme, some test requirements must handle ICs at lower speeds but with higher pad counts. Probing an array of dynamic-access-memory (DRAM) chips, for example, can increase the throughput of a test system significantly over individual die probing. High-reliability applications requiring known good die may require burn-in of parts. Contacting an entire wafer at once for burn-in is a challenge with on-wafer probing.

The Pyramid Probe Cards readily meet the challenges of high-density, high-speed IC testing. Each card features a replaceable membrane core with a contact-bump pattern customized to the IC under test. The two-layer metal thin-film membrane process supports a continuous ground mesh over the die, providing low 0.2-nH ground inductance that is comparable to the inductance of a flip-chip interconnection. Controlled impedance microstrip signal lines provide bandwidths to a maximum of 20 GHz, with wider bandwidth capability under development.

Precise control and repeatable production of the user-replaceable probe cores are achieved with lithographically-defined thin-film metal layers using processing steps similar to those used for IC manufacturing. The polyimide membrane is formed without tension into the distinctive pyramid shape. Low-impedance power contacts are routed to bypass chip capacitors mounted on the sloping sides of the pyramid (Fig. 2).

The Pyramid Probe Card is equipped with user-replaceable membrane cores that are durable and forgiving to use. The non-oxidizing nickel-alloy contact bumps (shown in the inset of Fig. 2) are long lasting with 1,000,000 contacts (touchdowns) guaranteed on gold pads.

Three different probe types make up the Pyramid family. The RF IC Pyramid Probe (Fig. 3) is used for microwave- and mixed-signal testing and can probe as many as 36 20-GHz-bandwidth lines or as many as 108 total input/output (I/O) contacts to a device under test (DUT). The low-cost Wireless Pyramid Probe (Fig. 4) has eight 3-GHz-bandwidth lines routed on the circuit board to SMA connectors and does not have any tooling charge as long as standard 50-Ω lines, power lines, and bypass capacitors are used. The LSI Pyramid Probe (Fig. 5) supports die sizes as large as 2.5 x 2.5 cm with as many as 532 signal lines with 1-GHz bandwidth or 132 RF lines with 3-to-10-GHz bandwidth.

Many standard probe-card configurations are available for the various Pyramid products, from standard 4.5-in. (11.43-cm) rectangular boards to 6-in. (15.24-cm) round boards. A wide
of the probe are low-impedance microstrip power-supply lines running to bypass capacitors located within 15 ps of the bond pads of the die. Both probing features support full device operating frequencies without oscillations or a significant power supply or ground bounce. Using the Cascade Microtech Pyramid Probe resulted in a 100-percent yield increase over probing the same wafer with a ceramic-blade card. The two major factors in the increase in yield were the mechanical issues of alignment and planarity, as well as electrical performance in ground inductance and bypass capacitors.

The largest GaAs device seen by Cascade’s engineers is a 25 x 15-mm gain and phase-modulation (PM) IC for controlling a phased-array satellite antenna. This application features a 3-GHz bandwidth with one RF input and 64 RF outputs. When 128 low-frequency control lines and grounds are added on both sides of all RF lines, the total pad count reaches 260 pads. Since this is a PM device, the probe card and cable lengths need to be matched within 15 deg., or approximately 15 ps.

For a propagation velocity of 150 µm/ps, the physical lengths need to be matched within 2.25 mm. This becomes a challenge for output pads that are distributed over the full length of the 25-mm side of the IC. It is possible to meander lines in the thin-film membrane to match lengths, but this becomes impractical for more than approximately 16 lines due to real-estate constraints. There are also design trade-offs between meandering as well as loss and signal integrity. Loss is dominated by resistive losses which scale with length. Controlling impedance is difficult in high-density meander patterns while the ground return path becomes more complex and may lead to increased crosstalk.

For this case, it was acceptable to lay out groups of lines matched within the 15-deg.
specification and provide a lookup table with their respective phase-matching within a group and between groups. This, along with a normal network-analyzer calibration scheme, works to support full functional testing on-wafer. Another approach to match 60 or even more than 100 lines within 10 ps is to characterize the membrane-core electrical lengths and then cut the semirigid coaxial lines to complementary lengths before assembling the probe card. This is labor intensive but may result in the best signal-integrity solution for complex applications.

The probe card for this application uses low-loss semirigid coaxial cable to route the 65 RF lines from the circuit-board membrane-probe core interface to the attached bulkheads. Attaching 65 SMA cables is labor intensive, but most customers are still specifying SMA cables due to their proven reliability, cost, and availability. Several high-density push-on high-frequency connectors are available for this application, but their acceptance is slow in the test environment despite their apparent improvement in setup times and ease of use. Low-frequency control lines are routed on the circuit board to Eurocard style 3 × 32 connector arrays.

The input on the left-hand side of this probe card is approximately 10 mm long and routed in coplanar waveguide. The bandwidth for this configuration is 10 GHz. The output lines are very long, about 30 mm, so they are routed in mesh ground microstrip with 80-µm-wide lines and approximately 20-percent ground mesh. This results in a 50-Ω line with 3-GHz bandwidth and DC resistance of less than 1 Ω.

Initial tests showed abnormally-low die-sort yields due to particulate contamination on the wafer in the 10-µm range caused by back-end wafer processing. Clean wafers resulted in high DC contact yields, but significant parametric failures occurred as expected on these large devices. The space-qualified package for this application is very expensive, so at-speed die sort results in large cost savings by reducing package scrap.

System optimization of the satellite has resulted in a new IC design with 32 channels, which is also used by the customer.

The initial Pyramid Probe product release three years ago was focused on the GaAs market, which is dominated by ICs with gold pads. The company has traditionally dominated this market and was a relatively-easy test bed since it is easier to make good low-resistance contact to gold pads than to aluminum pads. In just three years, the Pyramid Probe has become the industry standard for production testing of high-pin-count ICs with gold pads and more than 1-GHz bandwidth or low-inductance ground/power requirements. One-million-cycle contact life is guaranteed for contacting gold pads and it is extremely rare to wear out a probe. Typical use in production also indicates that these probes are much more robust and easier to use than other probe-card technologies. Several customers have actually moved their chucks and dragged their probe all the way across the wafer without damaging their Pyramid Probe.

The company has experienced an increasing demand for flip-chip die with solder bumps for RF ICs to be used in MCMs as well as growth in very-high-pin-count ASICs and microprocessors with up to 800 bumps. The primary driving force for these high-pin-counts is to minimize power and ground inductance as well as supply currents in excess of 30 A. Initial indications show that these demands are easily met, along with the added benefit of reduced solder-ball probe damage. Contact resistance studies are currently underway.

Dozens of high-speed communications IC designs with aluminum pads are routinely being tested in low-volume production and engineering evaluation, mostly in Japan. One recent customer evaluation has exceeded 200,000 touchdowns without performance degradation or visible wear. A preventive maintenance cleaning was performed only once at 100,000 cycles. Lifetimes in excess of 200,000 cycles are typical but many variables are still being evaluated, such as sensitivity to aluminum-alloy content, organic contamination, elevated temperature, and high current levels. The company is also developing standard cleaning and maintenance methods. New customer qualification is still managed very closely on a partnership basis. Customer partnering has made it possible for Cascade Microtech to offer a full-refund guarantee of complete customer satisfaction since product introduction; the company has not failed evaluation at a single customer site in three years.

Narrowing pad pitches, large arrays, and the necessity of testing 100 or more high-speed lines has stretched needle and blade technology to their limits. Pad pitches on certain devices are now at 70 µm and are rapidly moving to 50 µm (a pitch within the capabilities of the Pyramid Probe). For future microprocessors and ASICs with large-area arrays of more than 500 pads, needle- or ceramic-blade technology and buckling-beam technology will not support high-speed functional testing. In this area, a probe is being built for a high-speed microprocessor with more than 100 bypass capacitors located directly on the membrane within 35 ps of the die bond pad. As the cost, complexity, and size of devices increase, membrane technology should emerge as the viable solution for functionally evaluating such devices while still on wafer.

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Cascade Performance at a New Low Price

Cascade Microtech’s Pyramid Probe Cards are second generation membrane probes. The pyramid design allows: field replaceability, low-inductance bypass capacitors, short low-loss lines and controllable microscrub. And it doesn’t stress, stretch or deform. With Cascade’s Pyramid Probe Card you can:

• Reduce down time: 1,000,000 contacts possible
• Prove wafers at-speed in production: 
  Self-planarizing compliant core for easy operation
• Accelerate evaluation cycles
• Reduce package scrap and bond pad damage
• Provide customers with known-good-die
• Increase probe yield:
  Dimensional stability for repeatability and accuracy
• Minimize total cost of ownership

Cascade Microtech tackles your toughest measurement problems with an unbeatable combination: the most experienced technical support in the industry, and state-of-the-art probing systems, software, and probes. Cascade Microtech can help you stay ahead of the competition. And make a million bucks.

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