Integrated Wafer-Level Reliability Test System

Why Wafer-Level?
• The semiconductor industry relies on timely reliability test data to verify the quality of their product. On-wafer test provides this critical information faster than package-level testing, by eliminating the need for the dicing and packaging.
• On-wafer data is also high-integrity data – devices are not subjected to the potential mechanical or electrostatic stress during the packaging process.
• A complete wafer-level reliability (WLR) test system is simple to implement using a Cascade Microtech laboratory wafer prober, a Celadon probe tile platform, and an Aetrium Model 1164 reliability test system.

System Description
• A complete WLR test system includes:
  – Aetrium Model 1164 reliability test system with analysis software
  – Aetrium-Celadon wafer-level interface adapter kit
  – Celadon probe tile platform
  – Cascade probe station with thermal chuck
• This integrated WLR test system is capable of testing:
  – Copper and aluminum interconnects – electromigration (EM) and stress migration (SM)
  – Intra-level dielectrics (ILDs) – bias-temperature stress (BTS)
  – Gate oxides – time-dependent dielectric breakdown (TDDDB) and stress-induced leakage current (SILC)
  – MOS transistors – hot carrier injection (HCI), Vt stability, and negative-bias temperature instability (NBTI)

• This solution from Aetrium, Celadon, and Cascade features:
  – Multiple WLR applications
  – High capacity (using multi-site probe tiles) and parallel measurement system
  – Excellent signal integrity (with low-noise thermal chuck)
  – Mixed wafer-level/package-level test capability (using Notebook Ovens up to 450°C)
• This integrated system combines the expertise of three industry leaders to create one complete, high-performance WLR solution.
Aetrium Model 1164 Reliability Test System

Interconnects: 200mA 40V EM Modules or 80mA 5V EM Modules (16 DUTs per Module), EM/SM Analysis Software
ILDs, Gate Oxides: 40V 1mA Standard TDDB Modules (64 DUTs per Module) or 40V 350 mA High-Current TDDB Modules (48 DUTs per Module), SILC/TDDB Analysis Software
MOS Transistors: 15V 100mA/50mA/1mA (Channel/Gate/ Substrate) Standard HCI Modules or 12V 100mA/30mA/30mA Advanced HCI Modules (12 DUTs per Module), HCI/NBTI Analysis Software
Package Level: 300-mil, 600-mil, up to 28 pins
230°C, 350°C, 450°C Notebook Ovens

Celadon Ceramic Probe Tiles

Probe Platforms: Single-site and multi-site probe tiles (72mm, 114mm, 160mm, 220mm, and 320mm)
Probes: Up to 400 pins per probe tile, fA performance
Temperature: -65°C to +300°C, temperature-compensated across full range

Cascade Microtech Summit and S300

Automation: Semi-automatic, manual
Wafer Size: 4”, 5”, 6”, 8” (200mm Summit™ prober)
12” (300mm S300 prober)
Temperature: -65°C to +300°C
Microchamber*: Fast dry air purging for frost free cold temperature probing
Low-Noise Chuck: Super quiet wafer chuck to reduce substrate noise and transitions